

## REMARKS

Claims 1-19 are pending in the present application, were examined, and stand rejected. In response, Applicants amends Claims 6 and 18. Applicants respectfully request reconsideration of pending Claims 1-19, as amended, and in view of at least the following remarks.

### **I. Claims Rejected Under 35 U.S.C. §102**

The Patent Office rejects Claims 1-4, 6, 8, 10-16 and 19 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 5,884,057 issued to Blomgren, et al. ("Blomgren"). Applicants respectfully traverse this rejection.

Applicants respectfully assert that the Examiner has failed to adequately set forth a *prima facie* rejection under 35 U.S.C. §102(e). "Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*" Lindemann Maschinenfabrik v. American Hoist & Derrick ("Lindemann"), 730 F.2d 452, 1458 (Fed. Cir. 1994)(emphasis added). Additionally, each and every element of the claim must be exactly disclosed in the anticipatory reference. Titanium Metals Corp. of American v. Banner ("Banner Titanium"), 778 F.2d 775, 777 (Fed. Cir. 1985).

Claim 1 includes the following limitations which are neither taught nor suggested by either Blomgren or the references of record. Specifically, Claim 1 requires:

a first instruction set engine to process instructions from a first ISA having a first word size;

a second instruction set engine to process instructions from a second ISA having a second word size, the second word size being different than the first word size. [Emphasis added]

However, according to the Examiner, Blomgren teaches first and second instructions set engines to process instructions having a first word size and a second word size, the second word size being difference (sic) than the first word size. (Col. 6, lines 40-42) However, after having carefully reviewed the relevant portions of Blomgren cited by the Examiner, Applicants must respectfully disagree with the Examiner's contention.

Applicants submit that the teachings of Blomgren are limited to processing opcodes of different lengths. Applicants submit that there is no suggestion as to any variation in the word sizes between the RISC and CISC instruction sets within Blomgren.

Specifically, the Examiner's attention is drawn to the following quote from Blomgren:

The RISC and CISC instruction sets have independent encoding of instructions to opcodes. While both sets have ADD operations, the opcode number which encodes the ADD operation is different for the two instruction sets. In fact, the size and location of the opcode field in the instruction word is also different for the two instruction sets. Thus two instruction decoders are used for the two instruction sets – a RISC decoder 36 and a CISC decoder 32. (Col. 6, lines 37-44) [Emphasis added]

As indicated, CISC instruction sets and RISC instruction sets use independent encoding of instructions into opcodes. In addition, the size and location of the opcode field in the instruction word is different for the two instruction sets. Applicants submit that the cited passage implies that the instruction word size is the same for both the CISC and RISC instruction sets. Unless the CISC and RISC instruction words are the same size, Blomgren's indication of "the size and location of the opcode field in their instruction word being different for the two instruction sets" makes no sense. Accordingly, one skilled in the art would not interpret Blomgren as teaching instruction set engines for processing instructions from ISAs having different word sizes.

Furthermore, as known to those skilled in the art, a smaller number of opcodes are required to represent RISC instructions, as compared to CISC architectures, since CISC architectures include many additional instructions. However, this variation cannot support an argument that Blomgren teaches processing for instructions from a first ISA having a first word size different from the first word size and a second ISA having a second word size as required by Claim 1.

Accordingly, after carefully reviewing the entire text of Blomgren, Applicants respectfully submit that the Examiner's characterization of Blomgren is incorrect. Blomgren teaches a mechanism for rapid reconfiguration of pipeline alignment between a pipeline optimized for RISC instructions and one optimized for CISC instructions with the use of muxes and mode registers. (Abstract, and also as depicted with reference to Blomgren's Fig. 2)

Furthermore, as known to those skilled in the art, CISC instructions use memory operands, while RISC instructions use only register operands. (Col. 1, lines 47-51) Thus,

for RISC operations the pipeline is most efficient when memory access stages of the pipeline are located late in the pipeline, such as in the execute stage. However, for CISC operations the memory access stages must be located early in the pipeline before the execute stage so they can deliver a memory operand to the execute stage. (Col. 1, lines 50-55)

To this end, Blomgren describes various mechanisms for aligning the CISC and RISC pipelines, as depicted with reference to Figs. 2-3 and 5-7. Applicants submit that the entire description of Blomgren is devoid of any reference to providing processing for instruction sets

having different word sizes. However, the case law is quite clear in establishing that each and every element of the claim must be exactly disclosed in the anticipatory reference. Banner Titanium, id.

Accordingly, Applicants respectfully submit that the Examiner has failed to establish a *prima facie* rejection of Claim 1 under §102(e) in view of Blomgren. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §102(e) rejection of Claim 1.

### **Claims 2-4, 6 and 8**

Claims 2-4, 6 and 8 depend from Claim 1 and, therefore, include the patentable limitations of Claim 1, as described above. Accordingly, Applicants respectfully submit that the Examiner has failed to establish a *prima facie* rejection of Claims 2-4, 6 and 8 in view of Blomgren, as well as the references of record under §102(e). Accordingly, Applicants respectfully request that the Examiner reconsider and withdraw the §102(e) rejection of Claims 2-4, 6 and 8.

### **Claim 10**

Applicants respectfully submit that the Examiner has failed to establish a *prima facie* rejection of Claim 10 under §102(e) in view of Blomgren. Specifically, Blomgren fails to teach or suggest the limitations of:

fetching an input from at least one of a plurality of floating-point registers;  
detecting whether the input includes a token;  
if the token is detected in the input, checking what mode the processor is in.  
[Emphasis added]

Referring to Fig. 4 of Blomgren, floating point pipeline 14 reads floating point registers 20 during the F0 stage for register operands, and writes the result of the floating point operation back to the floating point registers 20 during the last stage. (Col. 7, lines 56-59) Furthermore, an additional port 25 into floating point registers 20 is provided from an integer pipeline 12 for memory operand loads and stores. (Col. 7, lines 50-52)

As a result, the contents of FP registers 20 is limited to memory operands for loads or stores for CISC instructions and register operands for floating point operations. Accordingly, Applicants respectfully submit that the detection of whether the input fetched from the floating point registers includes a token is neither taught nor suggested by Blomgren.

The Examiner directs Applicants to col. 6, lines 64-65 wherein,

the CISC instruction decoder 32 detects these emulated instructions and signals from unknown opcode over line 40 to mode control logic 30. In response, the mode control logic 30 sets RISC bit-60 in register 38 and loads the instruction

pointer with the address of the emulation routine in memory. Once the emulation routine is complete, an RISC instruction causes the mode register 38 to be reset to CISC mode and the instruction pointer updated to point to the following CISC instruction. The CISC program continues with the following instruction unaware that the instruction was emulated with RISC instructions. (See cols. 6-7 lines 61-10) [Emphasis added]

As is clearly indicated by the cited passage, there is no reference to whether a check of the processor mode is performed if a token is detected in the input, as required by Claim 10. However, the case law is quite clear that each and every element of the claim must be exactly disclosed in the anticipatory reference. Banner Titanium, *id.* Accordingly, although Blomgren describes emulation of certain CISC routines with RISC instructions, the processing performed within Blomgren does not vary according to the mode bit nor is there any determination as to the current mode in response to token detection.

Accordingly, Applicants respectfully submit that the Examiner has failed to establish a *prima facie* rejection of Claim 10 under 35 U.S.C. §102(e) in view of Blomgren or the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(e) rejection of Claim 10.

#### **Claims 11-16**

Claims 11-16 depend from Claim 10 and, therefore, include the patentable claim limitations of Claim 10, as described above. Accordingly, Applications respectfully request that the Examiner reconsider and withdraw the §102(e) rejection of Claims 11-16.

#### **Claim 19**

Applicants respectfully submit that the Examiner has failed to establish a *prima facie* rejection of Claim 19 under §102(e) in view of Blomgren. Specifically, Blomgren fails to teach or suggest the limitations of:

fetching an input from at least one of a plurality of floating-point registers;  
detecting whether the input includes at least one token of a plurality of  
tokens;  
if at least one token is detected in the input, checking what mode the  
processor is in. [Emphasis added]

Referring to Fig. 4 of Blomgren, floating point pipeline 14 reads floating point registers 20 during the F0 stage for register operands, and writes the result of the floating point operation back to the floating point registers 20 during the last stage. (Col. 7, lines 56-59) Furthermore, an

additional port 25 into floating point registers 20 is provided from an integer pipeline 12 for memory operand loads and stores. (Col. 7, lines 50-52)

As a result, the contents of FP registers 20 is limited to memory operands for loads or stores for CISC instructions and register operands for floating point operations. Accordingly, Applicants respectfully submit that the detection of whether the input fetched from the floating point registers includes a token is neither taught nor suggested by Blomgren.

The Examiner directs Applicants to col. 6, lines 64-65 wherein,

the CISC instruction decoder 32 detects these emulated instructions and signals from unknown opcode over line 40 to mode control logic 30. In response, the mode control logic 30 sets RISC bit-60 in register 38 and loads the instruction pointer with the address of the emulation routine in memory. Once the emulation routine is complete, an RISC instruction causes the mode register 38 to be reset to CISC mode and the instruction pointer updated to point to the following CISC instruction. The CISC program continues with the following instruction unaware that the instruction was emulated with RISC instructions. (See cols. 6-7 lines 61-10) [Emphasis added]

As is clearly indicated by the cited passage, there is no reference to whether a check of the processor mode is performed if a token is detected in the input, as required by Claim 19. However, the case law is quite clear that each and every element of the claim must be exactly disclosed in the anticipatory reference. Banner Titanium, *id.* Accordingly, although Blomgren describes emulation of certain CISC routines with RISC instructions, the processing performed within Blomgren does not vary according to the mode bit nor is there any determination as to the current mode in response to token detection.

Accordingly, Applicants respectfully submit that the Examiner has failed to establish a *prima facie* rejection of Claim 19 under 35 U.S.C. §102(e) in view of Blomgren or the references of record. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §102(e) rejection of Claim 19.

## **II. Claims Rejected Under 35 U.S.C. §103(a)**

The Patent Office rejects Claims 5, 7, 9 and 17-18 under 35 U.S.C. §103(a) as being unpatentable over Blomgren in view of IEEE Standard for Binary Floating-Point Arithmetic (hereinafter referred to as "IEEE").

In response, Applicants submit that Claims 5, 7 and 9 depend from Claim 1 and, therefore, include the patentable claim limitation of Claim 1, as described above. Furthermore, the Examiner's introduction of IEEE fails to provide any teachings relevant to first and second instruction set engines having either a first word size or a second word size, the second word size

being different from the first word size. Accordingly, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claims 5, 7 and 9 over Blomgren in view of IEEE.

#### Claim 17

Claim 17 depends from Claim 10 and, therefore, includes the patentable claim limitations of Claim 10, as described above. Furthermore, as described above with reference to Claim 1, Blomgren provides no teachings relevant to varying word sizes but simply provides reference to different opcodes for encoding CISC instructions as opposed to RISC instructions.

Accordingly, for at least the reasons described above, the Examiner fails to establish a *prima facie* rejection of Claim 17 under §103(a) over Blomgren in view of IEEE. Therefore, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 17.

#### Claim 18

Claim 18, as amended, requires a plurality of instruction set engines to process instructions from a plurality of ISAs having different word sizes. As described above with reference to Claim 1, Blomgren provides no teachings relevant to processing of instructions from ISAs having varying word sizes but simply provides reference to different opcodes for encoding CISC instructions as opposed to RISC instructions.

As indicated above, Blomgren teaches that the instruction words containing the RISC or CISC upcodes are the same. The differences, from the perspective of a decoder, is the location and size of the opcode within the instruction word. Accordingly, one skilled in the art would not interpret Blomgren as teaching instruction set engines for processing instructions from ISAs having different word sizes.

Therefore, for at least the reasons described above, the Examiner fails to establish a *prima facie* rejection of Claim 18 under §103(a) over Blomgren in view of IEEE. Consequently, Applicants respectfully request that the Examiner reconsider and withdraw the §103(a) rejection of Claim 18.

### CONCLUSION

In view of the foregoing, it is submitted that claims 1-19, as amended, patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

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By: 

Joseph Lutz, Reg. No. 43,765

12400 Wilshire Boulevard  
Seventh Floor  
Los Angeles, California 90025  
(310) 207-3800